REMARKS

Claims 1-5, 7-8, 10-18 and 35-54 are pending in the current application. Claims 1, 12 and14 are independent claims.

Drawing Objection

Figure 1 stands objected to under MPEP § 608.02(g) as lacking an appropriate legend. By the present Amendment, original Figure 1 has been replaced with replacement Figure 1, which includes the legend "Conventional Art". Accordingly, Applicant respectfully requests that the Examiner withdraw this objection.

35 U.S.C. § 112, 2nd Paragraph

Claims 36-37 and 47-48 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter set forth therein.

With regard to claim 47, Applicant has amended "the cache controller" to read as "a cache controller". Accordingly, Applicant submits that the antecedent basis informality has been corrected, and requests withdrawal of this rejection as it relates to claim 47.

With regard to claim 48, Applicant has amended "the plurality of DMA channels" to read as "a plurality of DMA channels. Accordingly, Applicant submits that the antecedent basis informality has been corrected, and requests withdrawal of this rejection as it relates to claim 48.

However, Applicant respectfully traverses this rejection as it applies to claims 36 and 37. Claim 36 is dependent upon claim 35, which depends upon claim 3, which depends upon claim 2. Claim 2 recites "a cache controller". Thus, Applicant submits that claim 36 and claim 37

(which depends from claim 36) includes sufficient antecedent basis support for the term "the cache controller". Applicant respectfully requests that the Examiner withdraw this rejection.

35 U.S.C. § 103(a) Volpe in view of Bourekas

Claims 1-5, 7, 10-13, 35, 38-40, 43-46, 49 and 52-54 were rejected under 35 U.S.C. § 103 (a) as allegedly being unpatentable over Volpe (U.S. Patent No. 6,895,475) in view of Bourekas (U.S. Patent No. 6,128,703). Applicant respectfully traverses this art grounds of rejection.

Volpe is directed to a prefetch buffer method and apparatus. The Examiner reads the claimed "processor core" upon core processor 10 of Figure 1 of Volpe, the claimed "cache memory" upon L1 data memory of Figure 1 of Volpe, and the claimed "on-chip memory" upon prefetch buffer 260 of Figure 3 of Volpe. Applicant agrees with the Examiner in that the prefetch buffer 260 fails to disclose "that the [prefetch buffer 260] is selectably filled with data from an external memory independent of the cache misses under user control" (See Page 5 of the Office Action). The Examiner alleges that Bourekas discloses this particular deficiency of Volpe.

Initially, Applicant directs the Examiner to Applicant's remarks filed along with the RCE of August 7, 2007. The Examiner does not appear to have provided remarks in response to Applicant's arguments provided in the above-noted response. Thus, as an initial matter, Applicant makes note of the technical deficiencies of Volpe and Bourekas, as well as the motivation of one of ordinary skill in the art to combine these references, and requests that the Examiner take these arguments into account in addition to the remarks provided below.

Bourekas is directed to a method and apparatus for memory prefetch operation of volatile non-coherent data. Generally, Bourekas teaches a cache-filling methodology wherein a programmer can selectively determine to ignore cache hits, such that data is retrieved from external memory irrespective of whether the retrieved memory is already located in the cache (see Bourekas, column 8, line 64 to column 9, line 2). Thus, for each cache access, the desired data is retrieved from external memory, regardless of whether that cache access results in a "cache hit" or a "cache miss".

As will be appreciated by one of ordinary skill in the art, the data retrieval of Bourekas, which can be configured to ignore cache "hits", is still entirely dependent upon a cache access of ***some*** type (i.e., a cache miss or cache hit) to trigger data retrieval from the external memory (see Bourekas, column 8, line 64 to column 9, line 2). Applicant directs the Examiner to presently pending independent claims 1 and 12, which have been amended to recite "wherein the on-chip memory is selectably filled with data from an external memory ***independent of cache accesses of the cache memory*** under user control" (Emphasis added). In view of the teachings of Bourekas as discussed above and the Examiner-admitted deficiencies of Volpe, Applicant respectfully submits that Volpe and Bourekas, either alone or in combination, cannot disclose or suggest the above-noted claim limitation.

As such, claims 2-5, 10-11, 13, 35, 38-40, 43-46, 49 and 52-54, dependent upon independent claims 1 and 12, respectively, are likewise allowable over Volpe in view of Bourekas at least for the reasons given above with respect to independent claims 1 and 12.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

35 U.S.C. § 103(a) Volpe in view of Bourekas in further view of Ramchandran

Claim 8 was rejected under 35 U.S.C. § 103 (a) as allegedly being unpatentable over Volpe (U.S. Patent No. 6,895,475) in view of Bourekas (U.S. Patent No. 6,128,703) in further view of Ramchandran (U.S. Publication No. 2004/0093479). Applicant respectfully traverses this art grounds of rejection.

Ramchandran is directed to a cache for instruction set architecture using indexes to achieve compression. A review of Ramchandran indicates that Ramchandran cannot cure the suggestion and disclosure deficiencies of Volpe in view of Bourekas as discussed above with respect to independent claim 1.

As such, claim 8, dependent upon independent claim 1, is likewise allowable over Volpe in view of Bourekas in further view of Ramchandran at least for the reasons given above with respect to independent claim 1.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

35 U.S.C. § 103(a) Volpe in view of Bourekas in further view of Kreitzer

Claims 41-42 and 50-51 were rejected under 35 U.S.C. § 103 (a) as allegedly being unpatentable over Volpe (U.S. Patent No. 6,895,475) in view of Bourekas (U.S. Patent No. 6,128,703) in further view of Kreitzer (U.S. Publication No. 2005/0025315). Applicant respectfully traverses this art grounds of rejection.

Kreitzer is directed to a method and apparatus for secure communications among portable communication devices. A review of Kreitzer indicates that Kreitzer cannot cure the suggestion and disclosure deficiencies of Volpe in view of Bourekas as discussed above with respect to independent claims 1 and 12.

As such, claims 41-42 and 50-51, dependent upon independent claims 1 and 12, respectively, are likewise allowable over Volpe in view of Bourekas in further view of Kreitzer at least for the reasons given above with respect to independent claim 1.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

35 U.S.C. § 103(a) Volpe in view of Bourekas in further view of Wing

Claims 14-18 were rejected under 35 U.S.C. § 103 (a) as allegedly being unpatentable over Volpe (U.S. Patent No. 6,895,475) in view of Bourekas (U.S. Patent No. 6,128,703) in further view of Wing (U.S. Patent No. 5,987,590). Applicant respectfully traverses this art grounds of rejection.

Initially, Applicant respectfully submits that Volpe in view of Bourekas cannot disclose or suggest "wherein the on-chip memory is selectably filled with data from an external memory ***independent of cache accesses of the cache memory*** under user control" (Emphasis added) as recited in independent claim 14. Further, Wing is directed to PC circuits, systems and methods. A review of Wing indicates that Wing cannot cure the suggestion and disclosure deficiencies of Volpe in view of Bourekas as discussed above with respect to independent claim 14.

As such, claims 15-18, dependent upon independent 14, are likewise allowable over Volpe in view of Bourekas in further view of Wing at least for the reasons given above with respect to independent claim 14.

Applicant respectfully requests that the Examiner withdraw the outstanding art grounds of rejection.

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, at the telephone number listed below.

Deposit Account Authorization

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

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Dated: January 25, 2008 By: /John Luigi Ciccozzi/

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